Docket No.: W&B-INF-1951

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : PETER BEER

Filed : CONCURRENTLY HEREWITH

Title : MEMORY CIRCUIT WITH A TEST MODE FOR WRITING TEST DATA

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

S i r :

In accordance with 37 C.F.R. 1.98 copies of the following patents and/or publications are submitted herewith:

Sugibayashi, T. et al.: "A Distributive Serial Multi-Bit Parallel Test Scheme for Large Capacity DRAMs", IEICE Trans.Electron., Vol. E77-C, No. 4, August 1994, pp. 1323-1327.

Respectfully submitted,

For Applicant WERNER H. STEMER
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Date: October 1, 2003

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FORM PTO-1449 (SUBSTITUTE) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT (37 CFR 1.98(b))	Attorney Docket No.: W&B-INF-1951 Appl. No.: Applicant: PETER BEER Filing Date: October 1, 2003 Group Art Unit:

EXAMINER INITIALS		PATENT NO.	DATE	PATENTEE	CLASS	SUB CLASS	FILING DATE
	A						
	B						
	C						
	D						
	E						
	F						
	G						
	H						
	I						

FOREIGN PATENT DOCUMENT

		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUB CLASS	TRANSL. YES	TRANSL. NO
	J							
	K							
	L							
	M							
	N							

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

		Sugibayashi, T. et al.: "A Distributive Serial Multi-Bit Parallel Test Scheme for Large Capacity DRAMs", IEICE Trans.Electron., Vol. E77-C, No. 4, August 1994, pp. 1323-1327

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.